

POWER EFFICIENT COMPACT APPROXIMATE MULTIPLIER FOR ERROR ROBUST APPLICATIONS USING REVERSIBLE LOGIC GATES

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Abstract:

The core purpose of approximate computing is to boost the system performance by optimizing the system parameters like power, delay and power delay product. This can be efficiently implemented where accuracy is not a key factor in many error tolerant applications like image processing, cryptography, embedded systems. In general, multipliers occupy 25-35% of the total circuit area hence becoming a fundamental block of any device. Therefore designing a well efficient multiplier can be of great use. In this study an approximate multiplier is designed employing a 4:2 compressor with reversible logic gates to reduce power and delay. The proposed architecture is simulated and synthesized using XILINX VIVADO and implemented using Zed board .

Index Terms: Approximate multiplier, reversible logic gates, compressor, and error tolerant applications

Introduction:

Approximate computing is a favorable approach to improve the speed and efficiency of the arithmetic circuits. To optimize the tradeoff between circuit performance and accuracy of the error tolerant applications like image processing and embedded systems this emerging technology has been employed. The main aim of the approximate computing is to enhance the circuit performance by neglecting certain input\output combinations which do not have adverse effect on the quality of the output.

Multipliers are divided into two types, one is exact multiplier which performs a binary multiplication and produces the result with full precession and the second one is approximate

multiplier which performs binary multiplication with some intentional error. The fundamental components of many complex circuits like multipliers, MAC units are compressors and full adders. Various application specific approximate compressor architectures have been proposed offering various advantages and disadvantages in the previous studies. The intermediate terms generated in the process of approximate multiplication are called as partial products. As a part of partial product reduction tree of a multiplier circuit, the compact approximate multipliers are typically constructed using alternative compressors and

full adders with lesser number of transistors. It is important to observe that existing approximate solutions with their large area requirements result in greater power usage and delay. Therefore optimizing the error rate and circuit parameters remains a vital challenge in compressors.

To address this critical issue, we propose novel approximate multiplier based on majority logic employed using reversible logic gates. Our proposed design uses 8 transistor circuit designed using reversible logic gates within the approximate PPRT sub circuit of a multiplier compared to the existing conventional 12 transistor circuit. Additionally we have designed a more accurate approximate multiplier using 14 transistors with reversible logic gates to further reduce the error rate. The efficiency of the proposed circuit is evaluated at the system level through the performance of the approximate multiplier in image multiplication. Further we have eliminated 15 AND gates in the PPRT stages by employing reversible logic and the number of exact compressors and partial products are also reduced. In this design we only require one exact compressor resulting in a total of 786 gates—achieving up to 49% area reduction and 93% energy savings compared to the exact multiplier. The evaluation highlights that each proposed and prior approximate compressor realizes a unique Boolean function and circuit topology, resulting in varied compromises between accuracy, power, and area.

II. Existing Method

Two approximate 4:2 compressors are proposed, highlighting the circuit efficiency over accuracy with reduced delay in [3][4]. The multiplier yields high accuracy and more area consumption because it consists of error recovery module (ERM) using hash tables which compute error distance (ED) in [5]. This multiplier in [13] displays increased area and high error rates. An adjustable multiplier with exact and approximate modes is designed in brief [6] showcasing higher area and up to 50% rise in output errors. In [7][8] using majority logic(ML) and CMOS

based circuits considerably minimizes area on the chip and power consumption to the disadvantage of increased error rates. The other methods are also designed as error control modules with algorithm based optimization in [11], probability based error correction [12] and approximate compressor based on circuit stacking [9] in all these techniques the area is increased optimizing the output errors.

III. Proposed Approach

There are prominently three steps in the multiplication process; the first one is partial product generation, followed by partial product reduction and lastly the final addition. The recent conventional compressors are designed using AND-OR and XOR logics, by utilizing these logic gates the dynamic power is notably intensified due to increased switching activity. Therefore to enhance the multiplier performance the partial product reduction stages are employed using reversible logic gates with majority

logic. In contemporary research the circuits employed using majority logic have shown higher design efficiency in comparison over the alternative approaches in the nano technologies. In this section a 4:2 approximate compressor is proposed using majority logic employed using reversible logic gates.

A. Dominant Logic:

To enhance fault tolerance, design simplicity and energy efficiency a dependable logic framework is employed which applies collective decision principle called as dominant logic (DL). This logic function generating a true output when more than half of its inputs are true or it generates a false output via odd input logic principle. DL based circuits traditionally require lesser number of gates due to the increased configurability. Hence, the compressors designed using DL based logic is a promising approach to reduce the circuit area without compromising on accuracy. The dominant logic takes multiple inputs and produces a single output.

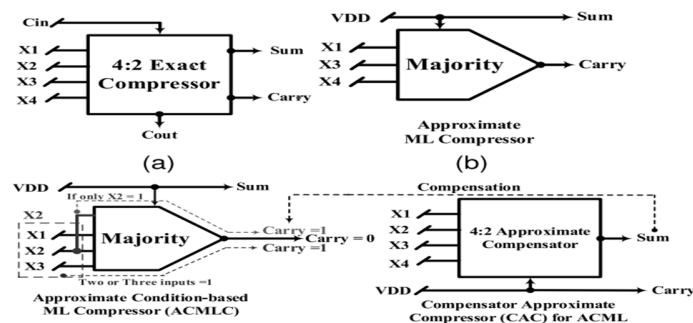


Fig: Schematic Representation of Majority Logic Using ACMLC

This logic gates can be operated as an AND gate or an OR gate by mapping one input to a constant logic value of either 1 or 0 respectively. The approximated bits are generated using DL based approximate components and transfer them to simplified circuits consisting of half adders(HA) and full adders(FA) with at least one input fixed. Initially dominant logic was effectively used in adders to minimize the circuit complexity and delay by remarkable amount. Therefore it is a good idea to blend approximate computing with dominant logic to provide notable advancements in system performance like area, power and delay especially in the designing of full adder circuit.

B. Reversible Logic Gates

Initially, reversible logic gates were employed in the field of thermo dynamics in which information processing done with irreversible logic generate huge amount of heat due to the loss of information. A logical arrangement of a circuit in which each input is mapped to each output and it can generate unique output combination for each input is called as a reversible logic gates. Note that the number of outputs is

same as the number of inputs. One of the prominent feature of reversible logic gates is whenever a primary input is generated which is not fed to the other gate as primary output it marks this input to the garbage value due to which the information loss can be controlled up to some extent.

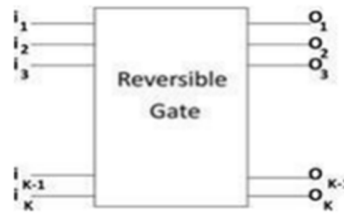


Fig: Block Diagram of Reversible Logic Gates

Minimum number of reversible logic gates should be used to design conventional reversible logic circuits. Reversible logic gates are crucial in quantum computing due to the fact that quantum mechanics works on the fundamentals of reversibility. After which these computations can be used in basic logic operations to save the data without any information loss and prevent the accumulation of errors. Some commonly used reversible logic gates from the previous researches include Fredkin gate, Peres gate, Feynman gate, Toffoli gate and Double Feynman gate.

C. Approximate State Based DL Compressor Using Reversible Logic Gates

To reduce area and improve performance dominant logic(DL) based compressors are majorly used, However traditional CMOS based compressor designs essentially suffer from information/data loss during state transitions due to which the heat dissipation increases according to the Landauer's principle. To counter this limitation we propose a reversible logic based implementation of dominant logic (DL) compressors, blending the error suppression feature of dominant logic with the power efficiency of reversible computing.

The main foundation of our design is the approximate state based dominant logic (ASDLC) and error compensated approximate compressor (ECAC). One should observe that DL based compressors take into account only three out of four inputs that is input x_2 is ignored and the output is fixed as $\text{sum} = \text{VDD}$. If at least two of the inputs are at logic '1' then the output carry is marked as true that is $X_1 + X_2 + X_3$ equals to two or three. This results in four positive errors and four negative errors. To decrease these errors and reduction in the area ASDLC compressor is proposed.

To add to this dominant logic compressor few more conditions are taken into considerations such as, We already know that the carry output is '1' when X_4 is ignored and $\text{sum} = \text{VDD}$, In addition

to this the carry output is 1 when (i) two of the three inputs are '1' (ii) only X2 is '1' rest all the inputs are '0'. By applying these conditions $\text{Sum (ASDLC)} = \text{VDD}$, $\text{carry(ASDLC)} = (X1.X3) + X2$. The simulation results of this Boolean function and reduction in the circuit area is shown in section IV.

An error compensator circuit is required to enable the information between exact and approximate sub circuits if a multiplier since approximate multipliers generates higher number of errors. To overcome this issue we propose an ECAC circuit which is based on a conventional 4:2 compensator design with carry fixed as $\text{carry} = \text{VDD}$ and sum is approximated as $\text{sum} = (X1.X2)(X3+X4) + (X3.X4)$. In general the energy dissipation in reversible logic gates is less which in turn reduces the power consumption compared to CMOS based DL circuits. Further dominant logic (DL) optimizes the intermediate stages of the multiplication process, shortening the critical path and yielding faster computation.

D. Architecture of Approximate 8-Bit Multiplier

Our proposed architecture of approximate multiplier consists mainly of three components constant truncation, approximation component and exact computation which are used to compute the partial products in stage1. The information loss is avoided in reversible logic which in turn reduces the power dissipation while reducing the gate count through truncation process of the least significant column. At least four LSB columns of partial products are truncated in a 8-bit multiplier while maintaining accuracy when combined with highly efficient reversible ASDLC based compressors.

In stage2 reversible ECAC gates are employed in the first and last column of approximate component to ensure output carry is preserved with minimal garbage value. For this reason more reversible AND gates are used to provide higher compression accuracy. In stage2 four additional reversible compressors are deployed in addition to the stage1 architecture while ignoring redundant inputs. As a result 49 reversible AND gates are only required eliminating 15 gates out of 64 irreversible AND gates. Here two reversible half adders and three reversible full adders are used to propagate the carry output from the ECAC circuit to the final addition stage without any loss of information.

Further moving to stage3 which employs ripple carry adders (RCA’S) with varying bit length is optimized using reversible compressors. With constant inputs sum=1 and carry=1 the proposed reversible ASDLC and ECAC circuits significantly reduce the number of half adders (HA) and full adders (FA) required. In the final stage in approximate component a reversible half adder (HA) is established with two fixed inputs of logic ‘1’ functioning equivalently as an inverter with no loss of energy. Further three more reversible full adders (FA) with constant input of logic ‘1’ are implemented using reversible XOR and OR gates respectively.

IV. Simulation Results

In this proposed brief, we are designing an approximate multiplier employing reversible logic gates with dominant logic. This was simulated using VIVADO XILINX under the supply voltage of 1.0v and clock frequency frequency of 100MHZ. The performance was analyzed in the terms of power consumption, delay and area and the results were compared with the traditional exact multipliers as well as previous work of approximate multiplier.

The simulation results and RTL view of proposed design are shown in figure.

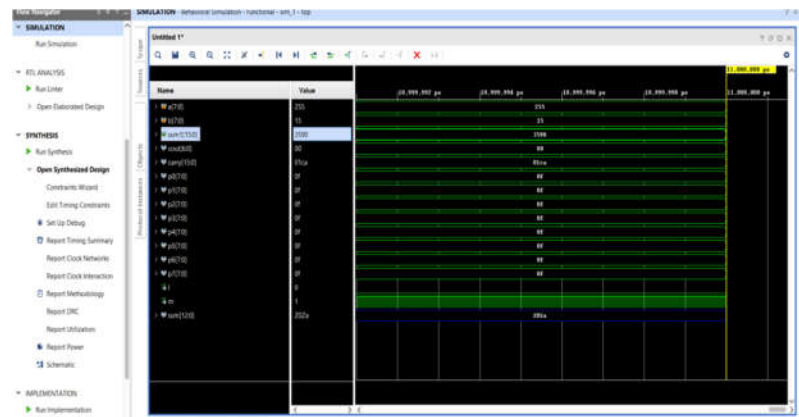


Fig: Simulation result of the approximate multiplier

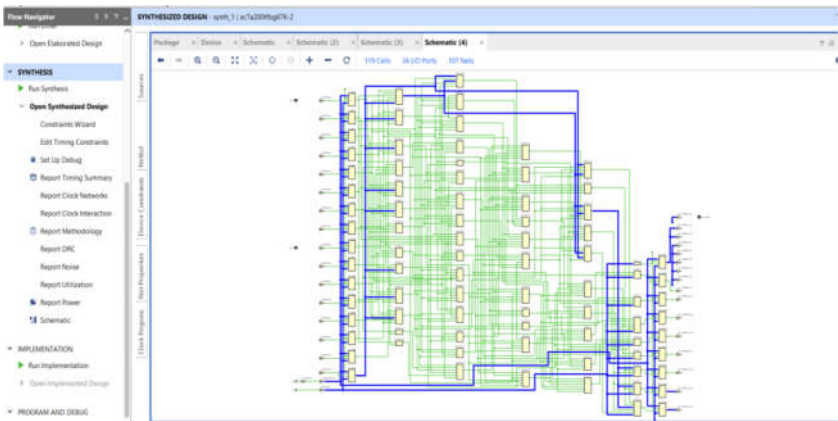


Fig: Schematic diagram of the approximate multiplier

A. Power Consumption

In software representation, Power usually refers to the computational resources required to perform the simulation including memory utilization and processing capability and other system resources necessary to model system behavior. The proposed method achieves a reduction of 1.058w power in comparison with the existing method which is 1.87w.

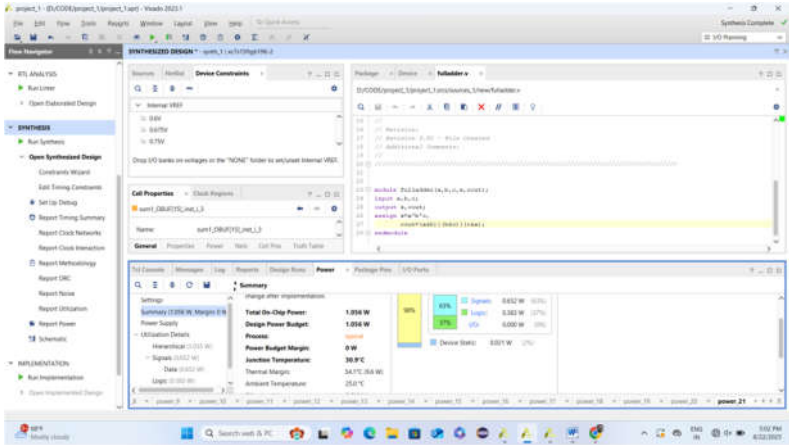


Fig: Power consumption report

B. Area Utilization

Area utilization illustrates the physical capabilities of the FPGA that are occupied by the synthesized and implemented design. Vivado reports these utilization metrics to help engineers analyze how effectively the available FPGA resources are being used which in turn facilitates

optimization with respect to performance, cost and power. By employing the proposed design there is a reduction of 45 LUTs in area compared to the existing method.

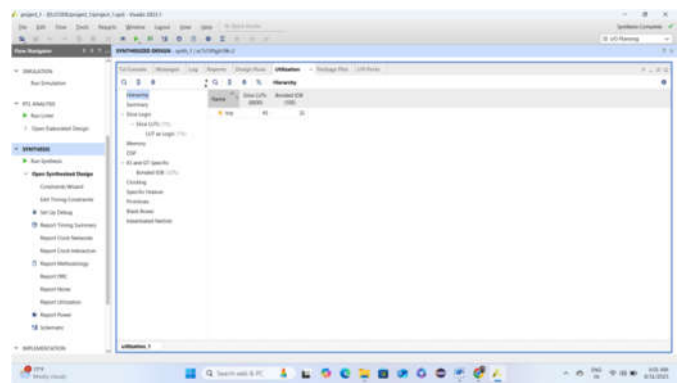


Fig: Area utilization report

C. Delay

The time taken for a signal to transmit through different parts of the simulated circuit is called as delay. It consists of many number of factors such as gate delay, inter connected delays and propagation delay which are caused by the performance of the digital components in any simulated design.

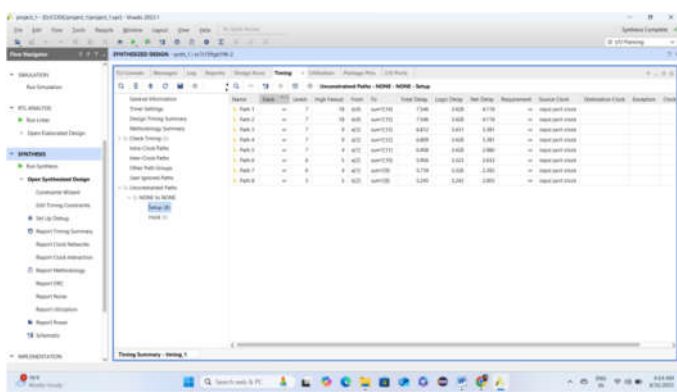


Fig: Timing report

V.Conclusion

In this paper, an 8-transistor ASDLC compressor, 14 transistors ECAC and an approximate 8-bit multiplier are proposed for precise and efficient multiplication. At the expense of high error rate the compressor has small imprints and low power consumption. We propose ECAC circuit to compensate for the generation of negative errors exhibiting seven errors with only one negative

error. We propose An ASDLC based approximate multiplier to utilize the proposed compressors unique characteristics. The proposed multiplier exhibits 41.5% area reduction and 43.4% power savings as compared to exact multiplier. Compared to state-of-the-art of approximate multiplier, the proposed multiplier exhibits higher performance across the most evaluated metrics. DL based proposed designs with reversible logic gates is a promising approach for low power and high performance applications in which accuracy is not of a big concern.

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