DESIGN OF LOW POWER 15-TRANSISTOR TRUE SINGLE-PHASE CLOCKING FLIP-FLOP

A. Victoria Amulya
M. Tech (VLSI &ES)
Student GPREC, Kurnool

W. Yameen
Assistant Professor, ECE Dept.
GPREC, Kurnool

ABSTRACT

In contemporary digital architectures, flip-flops serve as fundamental storage circuits and are extensively employed in pipeline registers and sequential modules. These elements contribute significantly to both overall power dissipation and chip area, making efficient designs crucial. This work introduces a 15-transistor true single-phase clocking (TSPC) D flip-flop optimized for low power consumption and high operating speed. The circuit integrates CMOS logic with complementary pass transistor logic, achieving reduced delay and simplified structure compared to conventional approaches. The proposed design was modelled and simulated in Cadence Virtuoso using the gpdk 45 nm technology library, operating at 1 V supply and 250 MHz clock frequency. Simulation results demonstrate power savings of up to 28%, a reduction of approximately 64% in clock-to-output delay, and a 15% decrease in layout area. These improvements highlight the suitability of the proposed architecture for compact, large-scale digital systems.

Keywords: TSPC, flip-flop, complementary pass transistor

EDA Tool: Cadence Virtuoso 6.16

Platform: Red Hat Enterprise Linux (RHEL) 8.8

1. INTRODUCTION

A flip-flop is a fundamental sequential circuit used to retain the logical state of one or more input signals in synchronization with a clock pulse. Within digital systems, these circuits are critical for managing operations in a defined sequence across successive clock cycles, acting as temporary storage elements that allow subsequent processing stages to function correctly. Depending on their configuration, flip-flops may sample inputs on either the rising or the falling transition of the clock edge. Those that respond to only one transition are classified as single-edge triggered flip-flops, whereas designs that respond on both transitions

are known as double-edge triggered flip-flops. It is worth noting that the clock distribution network in integrated circuits can account for nearly 20–40% of the total power.[1]

In modern VLSI circuits, random logic accounts for more than half of the overall power dissipation, with flip-flops contributing a substantial share of this consumption. Earlier generations of VLSI design primarily emphasized circuit performance and silicon area utilization, with manufacturing cost and reliability also considered essential. Power efficiency, however, was often treated as a secondary concern. In recent years, this perspective has shifted, and minimizing power usage has become a critical design target, alongside high speed and compact area. Portable devices, in particular, demand extended battery lifetime, which requires circuits to function with very low energy consumption. Likewise, reducing delay in storage elements is essential for achieving higher operating speeds. To address these needs, continuous innovation in flip-flop architectures has focused on low-power techniques. The Set–Reset flip-flop (SRFF) is among the traditional solutions, whereas the Transmission Gate flip-flop (TGFF) [2] has gained widespread acceptance in industry. A major limitation of both lies in heavy clock loading. These designs depend on two complementary clock signals (CLK and $CL\bar{K}$), which increase switching activity and raise transistor count. Moreover, the circuitry needed to produce the complementary clock adds further dynamic power consumption, even in cases where data activity is minimal. [3]

In modern VLSI design, controlling production costs and conserving chip area are increasingly important. As demand grows for smaller, more cost-efficient devices, reducing the silicon footprint of processors has become a major design goal. To lessen the burden on the clock network, various low-power flip-flop strategies have been introduced. One notable method is True Single-Phase Clocking (TSPC), which specifically addresses the issue of clock loading. Since excessive clock load can raise power consumption even when inputs remain unchanged, optimizing flip-flop structures is crucial for efficient design.

Additionally, flip-flops used in Application-Specific Integrated Circuits (ASICs) and real-time embedded systems must provide both high speed and low power consumption. As technology continues to scale down, there is an increasing need for innovative flip-flop designs that can function effectively at lower supply voltages.

2. LITERATURE REVIEW

To explore the basics of flip-flops, various conventional designs have been analysed. Standard SR flip-flops and Transmission Gate Flip-Flops (TGFFs) require additional circuitry to manage

clock signals. TGFFs, in particular, suffer from high clock loading since a single clock can control up to 12 transistors, leading to increased power consumption. To overcome these limitations, alternative designs such as the Adaptive Coupling Flip-Flop (ACFF), Topologically Compressed Flip-Flop (TCFF), and Logic Structure Reduction Flip-Flop (LRFF) have been developed.

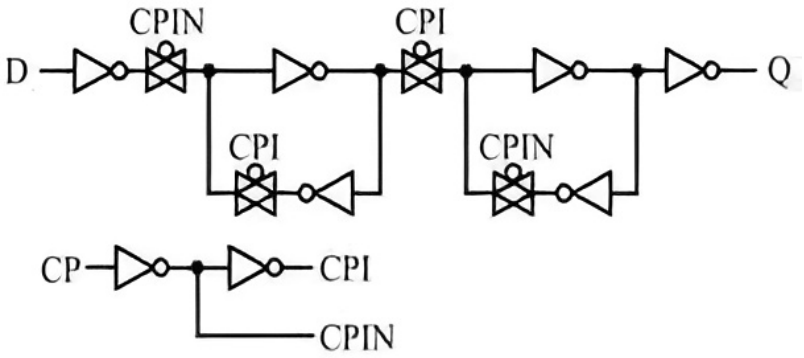

Fig.1. Transmission Gate Flip Flop

[4] In the Adaptive Coupling Flip-Flop (ACFF) design, a differential latch replaces the traditional SR latch to facilitate single-phase clock (TSPC) operation. Transmission gates are substituted with pass transistors, and two-level restoring (LR) circuits—each consisting of a parallel NMOS and PMOS pair are implemented. This configuration lowers clock loading because only four out of the 22 transistors are directly driven by the clock. Nevertheless, the slave latch in the ACFF is susceptible to data conflicts, and its efficiency decreases as switching activity rises.

[5] The Topologically Compressed Flip-Flop (TCFF) reduces the number of clock-driven transistors to only three, bringing the total transistor count to 21. This architecture offers a slave stage free from contention and is fundamentally based on the traditional SR latch. However, the TCFF is less suitable for high-frequency operation, as it acts like a transparent latch when the clock is low. Its pull-up strength also diminishes if the source voltage of transistor P2, elevated due to stacked devices, falls below the supply voltage. In this design, the SR flip-flop's master latch is replaced with a multiplexer, which reduces clock loading and supports a TSPC configuration. By employing topological compression, the TCFF achieves lower transistor count and reduced power consumption compared to the standard SR flip-flop.

[1] The Logic Reduction Flip-Flop (LRFF) is designed with a minimal 19-transistor structure, emphasizing reduced complexity but resulting in greater power consumption. Its architecture leverages complementary pass transistor logic (CPL), which divides the single

discharge path of the TCFF's slave latch into two separate routes. In this configuration, pass transistors controlled by the clock connect to intermediate sink nodes (node 2 and node 3). On the slave side, dual charging paths formed by CPL-based pass transistors allow nodes 4 and 5 to be pulled up to logic high, thereby improving performance. However, similar to the TCFF, the LRFF also suffers from a weakened pull-up effect, limiting its overall operational efficiency.

[6] The Adaptive Data Track Flip-Flop (ADTFF) is designed to be area-efficient while providing high-speed performance. It relies on a single clock input managed by four transistors, aiming to minimize both power consumption and propagation delay. However, due to voltage variations at its internal nodes, the ADTFF does not achieve significant improvements in either power efficiency or delay reduction.

Table.1 Comparison of Average Power, Clock-to-Output Delay, and Layout Area for Existing Flip-Flop Designs at 250 MHz and 1 V

Flip Flops	**Topologically Compressed Flip Flop (TCFF)**	**Logically Reduced Flip Flop (LRFF)**	**Adaptive Data Track Flip Flop (ADTFF)**
Number of Transistors	21	19	18
Average Power(µw)	2.43	2.32	1.96
Clock-Output delay(ps)	144.17	138.63	139.09
Layout Area(µm)^2	31.56	30.42	28.61

In summary, multiple flip-flop architectures have been developed to address the shortcomings of conventional SR and Transmission Gate Flip-Flops (TGFFs), particularly their high clock loading and power demands. The Adaptive Coupling Flip-Flop (ACFF) lowers clock-driven transistor count by employing a differential latch and pass transistors, but it is prone to data conflicts and its performance declines under high switching activity. The Topologically Compressed Flip-Flop (TCFF) limits clock-driven transistors to three and replaces the master latch with a multiplexer, reducing both power consumption and transistor count; however, it encounters challenges at high frequencies and exhibits weaker pull-up

strength. The Logic Reduction Flip-Flop (LRFF) decreases the transistor count further to 19 through complementary pass transistor logic (CPL), which enhances performance but increases power usage and retains pull-up limitations. Finally, the Adaptive Data Track Flip-Flop (ADTFF) provides high-speed operation and compact area with minimal clock control, yet internal voltage fluctuations restrict its improvements in power efficiency and delay.

3. PROPOSED FLIP FLOP

To achieve lower delay, simplified circuitry, and improved power efficiency, the master-slave portion of the proposed flip-flop is designed using the adaptive data track approach. The structure consists of 6 NMOS and 9 PMOS transistors. To prevent excessive clock loading, the flip-flop uses a single clock signal, with only four NMOS transistors directly driven by the clock input.

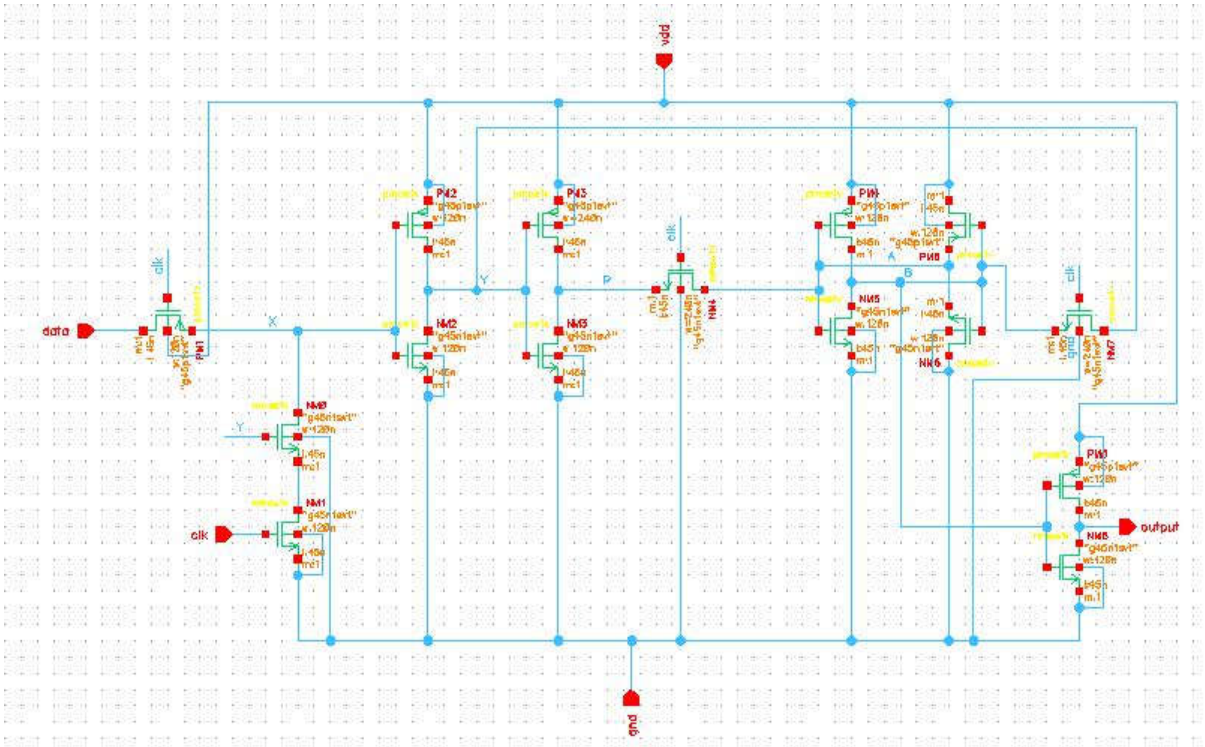

Fig. 2. Proposed Flip-Flop Design

The proposed flip-flop design incorporates an adaptive mechanism for data retention and signal propagation, aiming to improve reliability, reduce power usage, and increase operational speed compared to traditional designs. A notable aspect of this approach is the inclusion of charge keeper transistors N5 and N8, which have been widened to enhance their charge-holding ability. This modification ensures that the stored data remains stable despite leakage currents, thereby improving data retention and lowering the risk of data loss.

Performance is further enhanced through the strategic use of pass transistors. These transistors enable efficient data transfer between the master and slave stages and help lower overall power consumption by limiting unnecessary switching events.

Isolation is provided by transistor P1, which separates the master stage from input changes when the clock is high, preventing data corruption and maintaining stability at key storage nodes X and Y. Transistor N2 helps preserve the stored data at these nodes, while N1, connected in series with N2, reinforces the data retention capability at node X.

The architecture uses four clock-driven transistors—N2, N5, N8, and P1—to achieve efficient synchronization while minimizing clock load. The widths of N5 and N8 are intentionally increased to enhance drive capability, allowing faster signal transitions and more robust propagation to the slave latch.

Finally, transistors P4, P5, N6, and N7 function as static storage elements, guaranteeing that data remains reliably held in the slave stage until the subsequent clock cycle. The integration of keeper transistors, isolation circuitry, and carefully optimized pass transistors together improves the proposed flip-flop's speed, stability, and power efficiency.

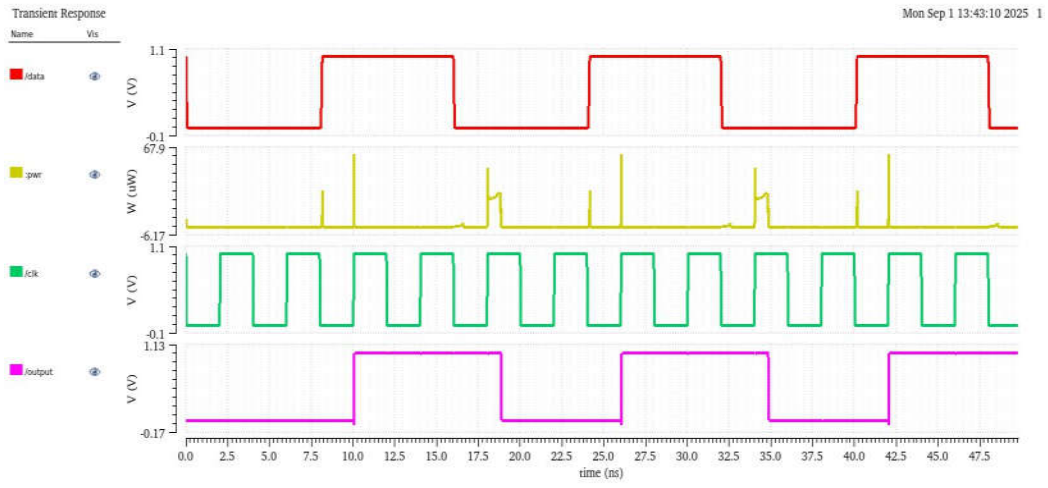

Fig. 3. Signal Waveform of the Proposed Flip-Flop

4. COMPARISION OF PARAMETERS

In this section, simulations are performed for the TCFF, LRFF, ADTFF, and the proposed 15-transistor flip-flop using GPDK 45 nm technology. The performance is assessed based on key metrics such as average power consumption and clock-to-output delay. The evaluation assumes a supply voltage of 1 V and an operating frequency of 250 MHz.

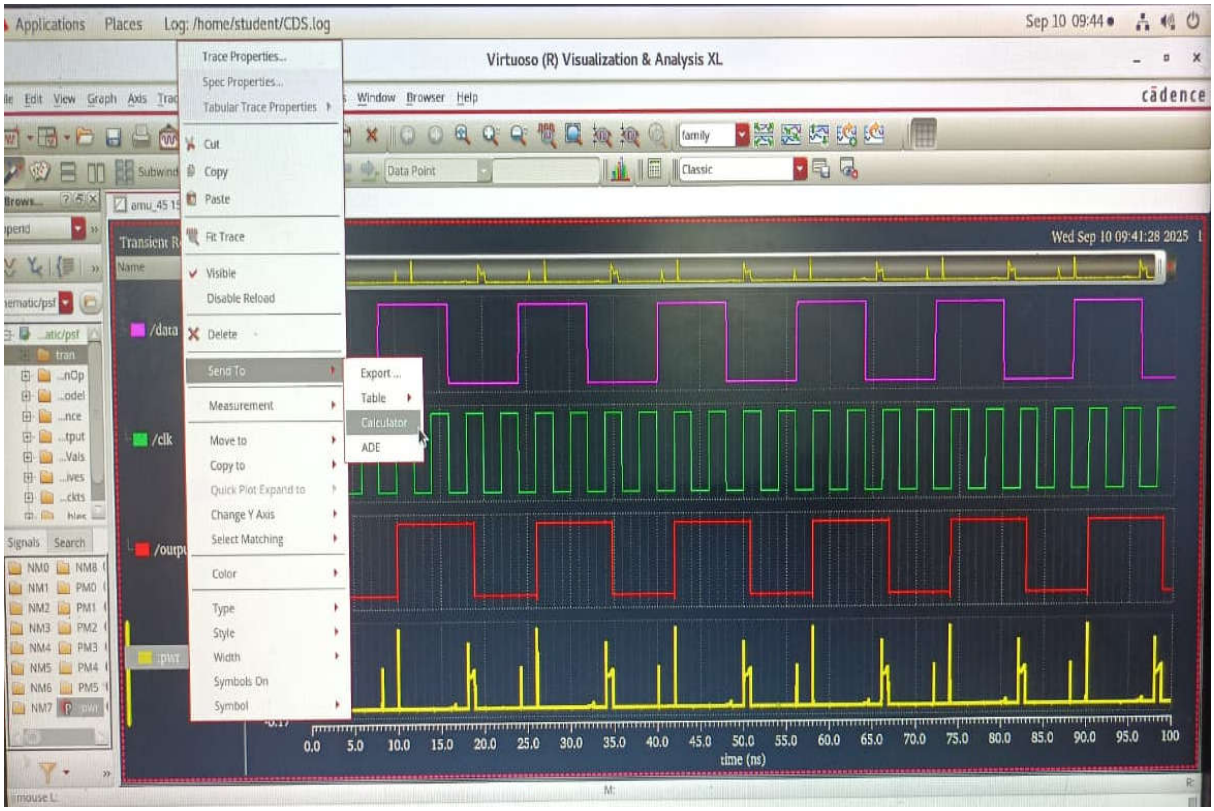

Fig.4 Power Waveform

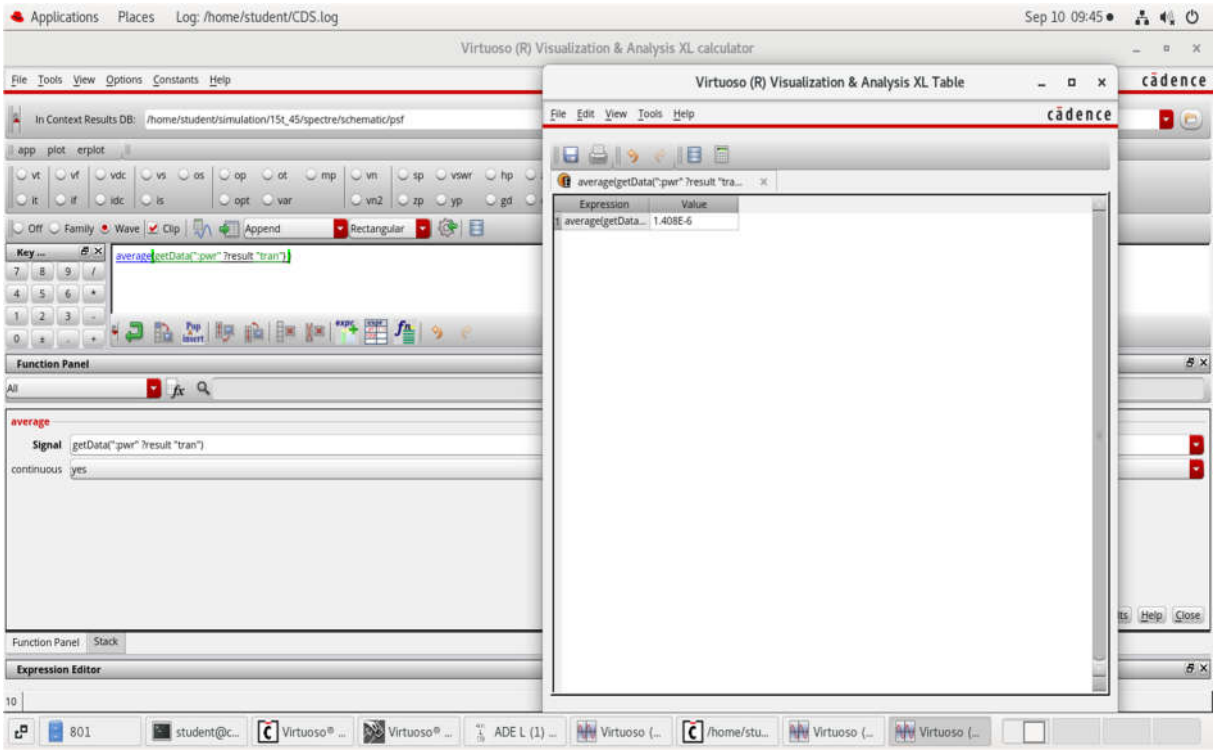

Fig.5. Computation of Average Power for the Proposed 15T Flip-Flop

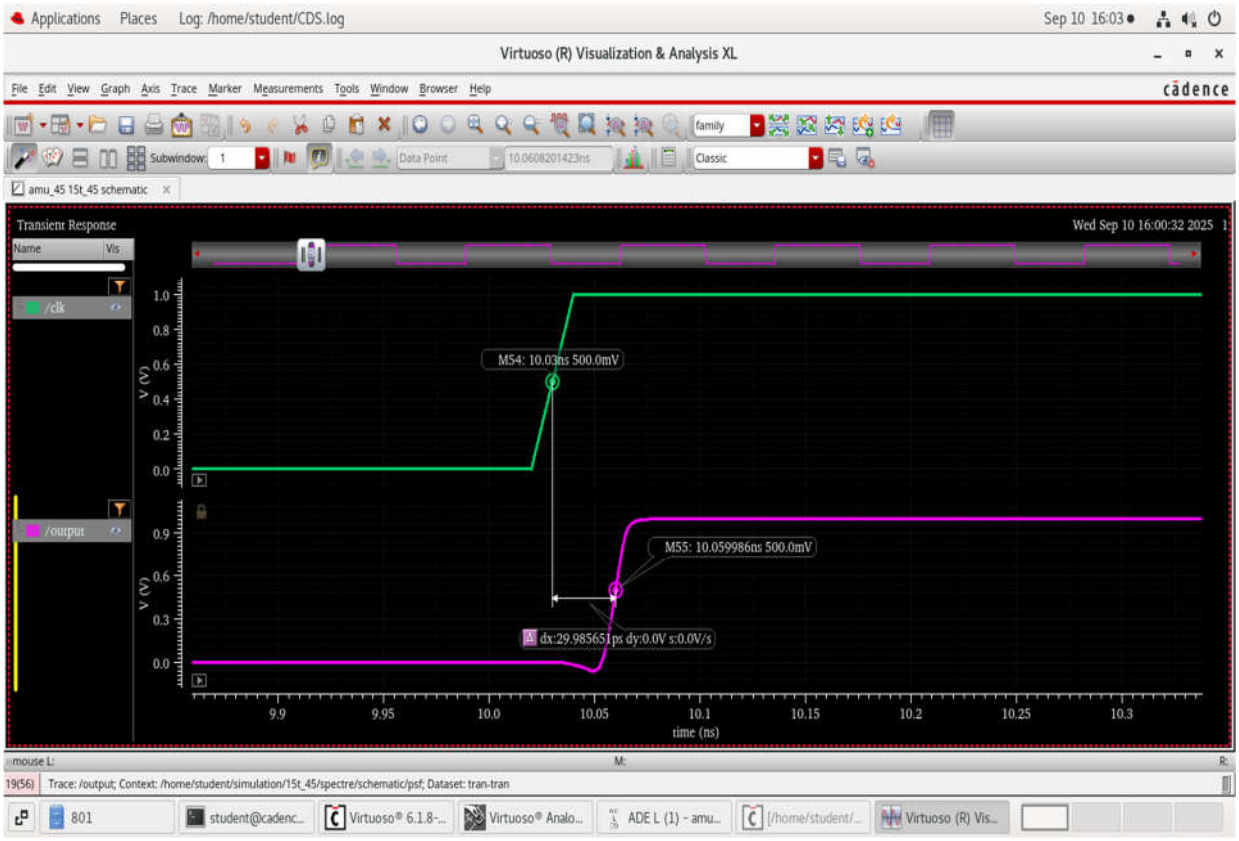

Fig.6 Evaluation of Clock-Output Delay in the 15-Transistor Flip-Flop

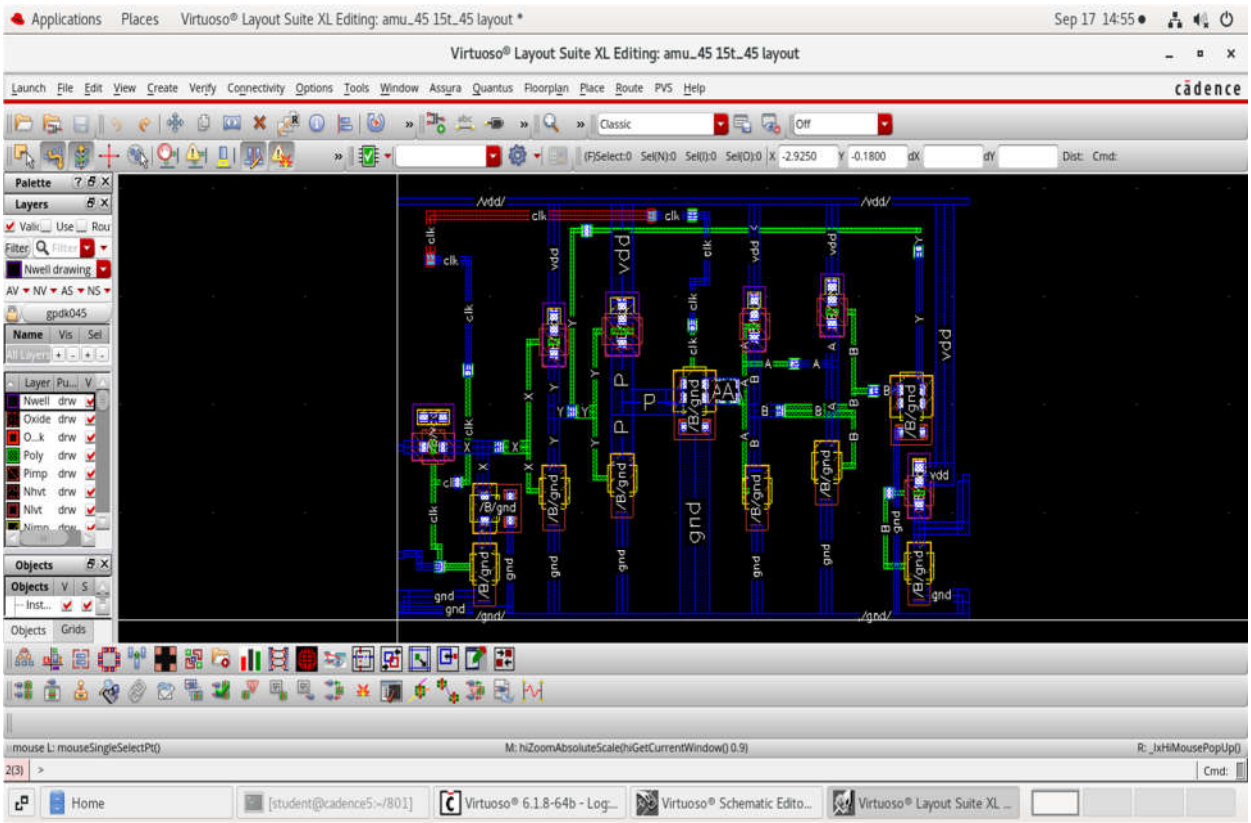

Fig.7 Circuit Layout Representation of the 15-Transistor Flip-Flop

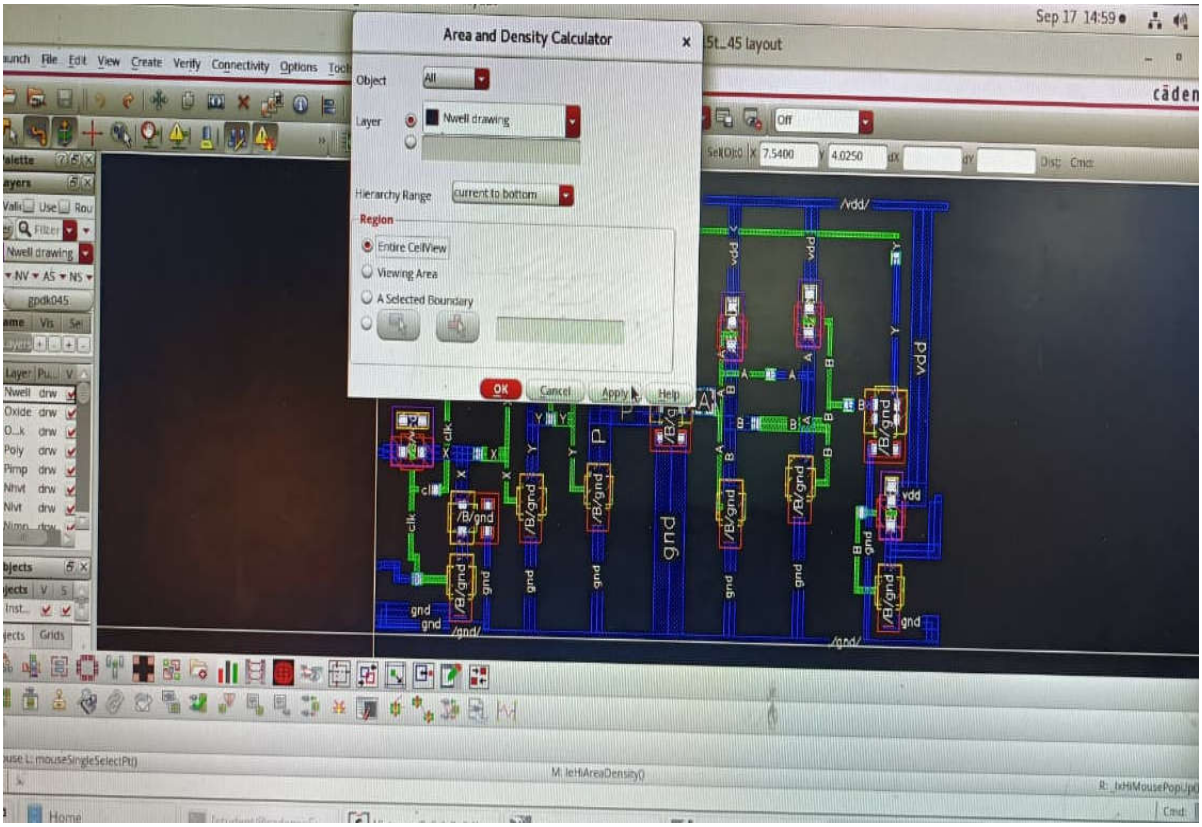

Fig. 8 Layout Area Estimation

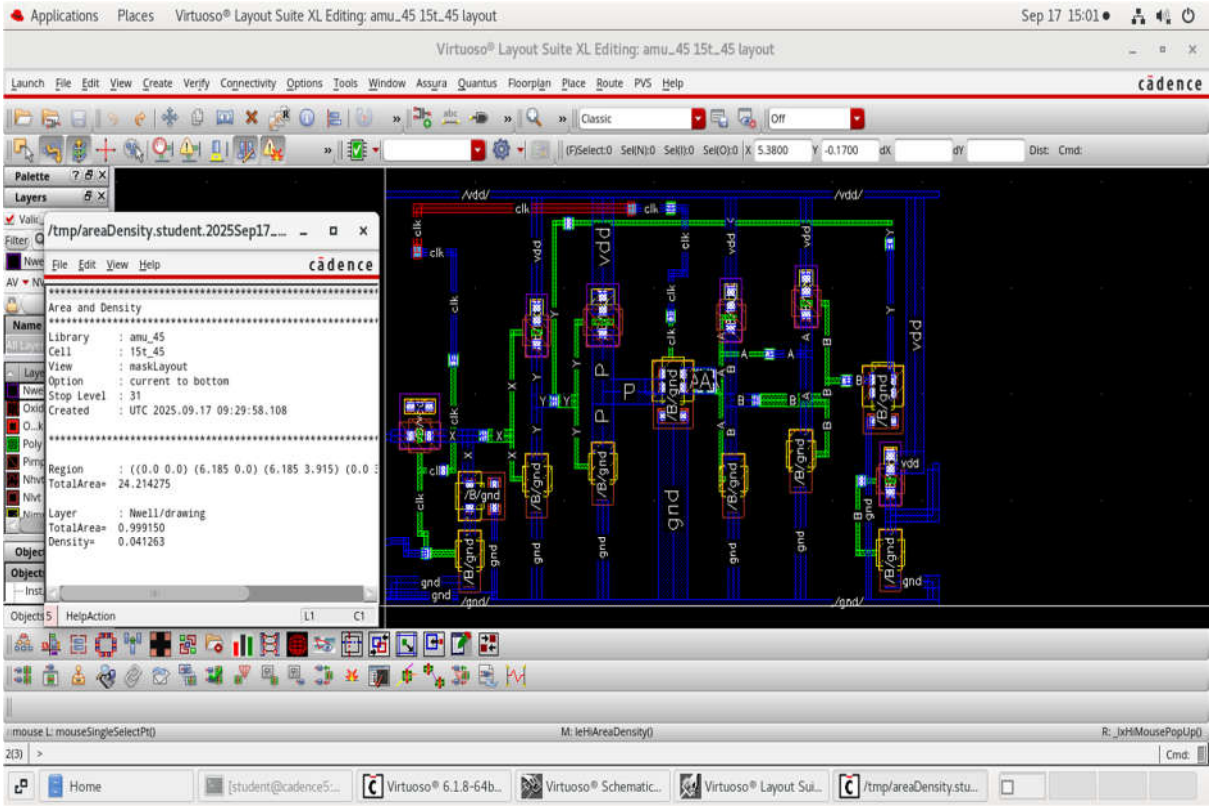

Fig. 9 Calculated Layout Area Window

Table.2 Comparison of Average Power, Clock-to-Output Delay, and Layout Area for Proposed and Existing Flip-Flop Designs at 250 MHz with 1 V Supply

Flip Flops	TCFF [5]	LRFF [1]	ADTFF [6]	Proposed Flip Flop Circuit
Number of Transistors	21	19	18	15
Average Power(µw)	2.43	2.32	1.96	1.40 (28% better)
Clock-Output delay(ps)	144.17	138.63	.83.94	29.9 (64% better)
Layout Area(µm)^2	31.56	30.42	28.61	24.21 (15%better)

5. CONCLUSION

A novel 15-transistor True Single-Phase Clocking (TSPC) flip-flop has been developed, offering both low power consumption and high-speed operation. The design reduces the transistor count, thereby minimizing the required chip area. Compared to existing flip-flops, the proposed design demonstrates superior performance in terms of both area efficiency and power savings. It operates effectively across a range of frequencies up to 2 GHz, making it well-suited for high-speed applications such as GHz-range processors and counters.

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